INVESTMENT MEMORANDUM

High Bandwidth Flash: Mapping the Chain, Pricing the Shock

An investment memorandum on the companies connected to HBF, the second-order NAND supply thesis, and where the opportunity actually sits

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Authorship, expertise, and method. Shimogoryo Base LLC is owned and operated by **Andy Kowles**, its Principal Analyst and the author of this memorandum. The work began not with a prompt but with his own sustained research into **memory and storage tiers optimised for AI inference**, which produced the thesis this memorandum rests on — that HBF should be modelled on how HBM disrupted DRAM microeconomics, and that the effect would prove larger. **Only after that thesis existed** were frontier large language models engaged, as directed instruments: the underlying research report was compiled through a custom Fable 5 agentic loop specified and operated by Shimogoryo Base LLC/GK, used for retrieval at scale across a fragmented public record. Every load-bearing claim was then **live-verified against primary sources** on 8–9 July 2026 and the result **hand-reviewed and hand-edited** by the analyst. Sequence matters: domain expertise, then thesis, then machine-assisted research, then verification, then human judgment. See *"5. How this memorandum was made"* for the full account.

What is original here. The wafer-diversion model in Section 2 is **original work of Shimogoryo Base Consulting**, published here for the first time. The SLC-versus-TLC density penalty is taken directly from the underlying report; the array-efficiency, TSV keep-out, and known-good-die penalties are the analyst's own estimates, presented as a low/base/high range precisely because they are estimates. Market prices, market capitalisations, and multiples referenced are as of late July 2026 and will have moved. Company classifications reflect the Publisher's judgment about supply-chain position, not any assessment of investment merit.

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Bottom line

The report identifies roughly thirty companies with economic exposure to HBF. Almost every obvious one has already made its move — SanDisk is up 3,294% in twelve months, Micron has crossed a trillion dollars, Kioxia is up around 800%, and Western Digital and Seagate sit at record highs. None of that was caused by HBF. It was caused by the 2026 memory shortage, and HBF has generated no revenue at all.

That gap is the entire opportunity. HBF's real financial significance is a supply-destruction mechanism that this memo quantifies for the first time: an HBF wafer yields roughly 5.6x fewer sellable bits than a commodity TLC wafer, which is about 2.4x more violent than HBM's effect on commodity DRAM. The working hypothesis behind this memo was right, and understated.

But it lands in 2029-2030, not now. So the actionable positions are not the NAND makers at cycle-peak multiples. They are the suppliers levered to wafer starts, bonded interfaces, test insertions, and the HBF controller IP that does not yet exist — none of which carry any HBF premium today.

1. What the report actually says, in one page

High Bandwidth Flash stacks 3D NAND dies with through-silicon vias over a base logic die, in HBM's physical idiom, and drops the result into an HBM site on the same 2.5D interposer as the accelerator. SanDisk introduced it in February 2025, SK hynix co-signed a standardisation MoU in August 2025, and in February 2026 the two converted that into a formal consortium under an Open Compute Project workstream.

The pitch is 512GB per stack at 1.6TB/s read — roughly 8 to 16 times HBM's capacity per stack at comparable cost per stack, with microsecond rather than nanosecond latency. It is a read-mostly tier: model weights, reusable prefix and KV caches, embeddings, RAG corpora. It complements HBM rather than replacing it, and SK hynix — the HBM leader — co-signing is the strongest evidence of that framing.

Three things in the report matter far more to an investor than the headline specs, and they are the spine of everything that follows.

First: HBF requires unique wafers, and they are terrible wafers

This is Section 3, and it is the most financially consequential passage in the document. An HBF core die inverts every priority of a commodity NAND die. Plane count rises 10 to 50 times, with sense-amp and page-buffer area to match, trading array efficiency for bandwidth. TSV corridors must be punched through a 200-to-400-layer array. The media is SLC, which costs three times the density of TLC immediately. Each array wafer consumes a bonded CMOS wafer on an advanced-ish logic node.

The report draws the conclusion explicitly and tells you what to do with it: "HBF NAND will be economically disruptive, and the author recommends using the HBM disruption of DRAM microeconomics as a model."

Second: the fight is over shoreline, not silicon

HBF's key strategic compromise is that it occupies existing HBM sites rather than demanding new beachfront. That converts adoption from "will xPU vendors redesign for flash?" — which they would not — into "how many HBM sites is a terabyte worth?", which is an arithmetic question about inference token economics. It is why HBF is credible where Optane was not.

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Third: the timeline is genuinely 2028

Samples in the second half of 2026, first inference device samples in early 2027, first meaningful revenue silicon in 2028, mainstream attach 2029-2030. KAIST's Prof. Joungho Kim independently predicts late-2027 to early-2028 commercialisation. No xPU design win had been publicly disclosed as of the report's July 2026 verification. Anyone telling you HBF explains a 2026 stock move is selling something.

2. The wafer diversion model — quantifying the NAND question

The question this memorandum was built to answer is whether HBF does to NAND what HBM did to DRAM. The mechanism in both cases is identical: a premium product consumes wafer starts while yielding far fewer sellable bits, so merchant supply falls faster than wafer capacity does, and the market is pushed out of supply-demand equilibrium. The difference is magnitude, and HBF's magnitude is larger.

2.1 Bits destroyed per HBF wafer

Penalty factor	Low	Base	High	Basis
SLC vs TLC cell density	3.00x	3.00x	3.00x	Report Sec 2.3, stated exactly. Not an estimate.
Array-efficiency loss from mini-plane subdivision	1.25x	1.45x	1.70x	Report Sec 2.1-3.1: plane count 10-50x higher, "more periphery per bit". Magnitude estimated.
TSV keep-out corridors	1.05x	1.10x	1.18x	Report Sec 3.1: array must be partitioned around TSV corridors. Estimated.
16-high stack and KGD yield loss	1.10x	1.18x	1.35x	Report Sec 2.4. NAND carries bad blocks, so KGD screening discards more. Estimated.
COMPOUND PENALTY	**4.33x**	**5.65x**	**8.12x**	**Multiplicative.**

For comparison, the same exercise on HBM — DRAM die area roughly 1.6-2.2x commodity DDR5 plus 1.15-1.40x stacking and KGD yield loss — compounds to about 2.4x at base case. HBF is therefore roughly 2.4 times more destructive of merchant bits per wafer diverted than HBM was.

2.2 What that does to merchant supply

Scenario	HBF share of NAND wafer starts	Merchant bit supply lost vs no-HBF counterfactual	Plausible year
Pilot and samples only	0.2%	0.9%	2027
First inference devices ship	0.8%	3.7%	2028
Mainstream inference attach	3.0%	13.9%	2029-2030
Bull case — HBF becomes standard	6.0%	27.9%	2030+

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> **The number that matters**
>
> Goldman Sachs put the 2026 DRAM supply-demand gap at 4.9% and called it the most severe shortage in fifteen years. NAND contract prices are up more than 100% cumulatively in the first half of 2026 on that kind of imbalance.
>
> At the mainstream-attach scenario, HBF removes roughly 14% of merchant NAND bit supply against the counterfactual — about three times that proportional shock, from a single product line consuming only 3% of wafer starts.
>
> That is why the report's phrase "economically disruptive" is not marketing. It is arithmetic.

Two honest caveats. The 3% adoption assumption is a scenario, not a forecast — no public estimate of HBF wafer share exists and none of the numbers in the middle column of the first table above are disclosed by anyone. And the effect is 2029-2030. Today's price surge has nothing to do with HBF. Conflating the two is the single easiest way to lose money on this thesis.

3. What the full memorandum covers

This is an **abridged edition**. It carries the whole argument — what the technology is, the wafer-diversion model that quantifies the supply shock, the conclusion, and the method behind it — but not the name-by-name work. Four sections are held back:

- **The company map.** Thirty-one US-listed names sorted into three tiers: direct participants (SanDisk, SK hynix ADR, Kioxia ADR, Micron, Samsung), the deeper supply chain that gets paid at design-in and pilot-line construction (bonding, wafer, controller, and inspection/metrology exposure), and the price-umbrella beneficiaries who simply sell into a tighter NAND market.
- **Ranked opportunities.** Five names scored on HBF leverage, exposure purity, valuation headroom, and timeline fit, each with the specific mechanism, the entry problem, and the risk that breaks it — plus the second thesis on the NAND price umbrella.
- **The SanDisk problem.** Why the most correct name is also the most dangerous, and how to read a forward multiple of 8 after a 33x move.
- **What would kill this, and the tripwires.** The falsification criteria, and a dated watch list of events that would confirm or break the thesis between now and 2028.

Those sections, together with the companion workbook `HBF_Investment_Screen.xlsx` — the full grid with per-name evidence, exposure estimates, market data, and bull/bear cases — and the underlying research report are available from the Publisher at shimogoryobase.com/consult.html.

4. Summary

The report describes a technology that is credible, demand-pulled, evolutionary in every component, and strategically well-designed in reusing HBM's shoreline. It is also three years from revenue, has no disclosed customer, and depends on two vendors persuading three more to join them.

The investable content divides in two, and they should not be confused. The direct HBF thesis is real but early, and the way to own it is through the suppliers who get paid at design-in and pilot-line construction — controller IP, bonders, test, materials — rather than through the memory makers who get paid in 2029. The second-order NAND pricing thesis is real, larger than the HBM precedent, and quantified here at roughly three times the proportional supply shock that produced the worst DRAM

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shortage in fifteen years — but it arrives in 2029-2030 and is not what is driving today's prices.

The mistake to avoid is the natural one: reading this memorandum, seeing that HBF will tighten NAND, and buying NAND equities that have already tripled or worse on an entirely different catalyst. The wafer math is a 2029 argument. Buying it at 2026 cycle-peak multiples means being right about the mechanism and losing money anyway.

All forward-looking assessments here are uncertain, and the wafer-diversion model rests on estimated inputs that are labelled as such in both this memorandum and the companion workbook. Market data is as of the dates shown, was collected from public financial media, and must be independently verified against a live feed before any action is taken. Prices and multiples in a cyclical industry at a cycle peak can change very quickly.

5. How this memorandum was made

Buyers of research are entitled to know who did the thinking, in what order, and with what instruments. The short answer is that the domain expertise came first and the machines came second.

The analyst. Shimogoryo Base LLC is owned and operated by **Andy Kowles**, who serves as its Principal Analyst and is the author of this memorandum and of the underlying research report. Shimogoryo Base is his firm; the judgments in this document are his, and he is accountable for them.

Expertise first. The HBF work did not begin with a prompt. It began with a sustained, independent research programme into **memory and storage tiers optimised for AI inference** — the economics of the HBM stack, the microeconomics of NAND wafer allocation, packaging and bonding constraints, and the shoreline arithmetic that governs what can actually sit next to an accelerator. That programme produced the analyst's own working thesis about High Bandwidth Flash, including the central analogy on which this memorandum turns: that HBF should be modelled on *how HBM disrupted DRAM microeconomics*, and that the disruption would prove larger. The hypothesis, the framing, and the questions worth asking were formed **before** any model was engaged.

Then the instruments. Only once that thesis existed were frontier large language models brought in — deliberately, and as instruments under direction. The underlying research report was compiled through a **custom Fable 5 agentic loop** specified and operated by Shimogoryo Base LLC/GK, tasked against vendor disclosures, conference material, trade press, and academic literature. The models did what they are good at: retrieval at scale, systematic canvassing of a fragmented public record, structured drafting, and holding thirty-odd companies and their supply-chain relationships in view at once. What the models were *not* asked to supply was the thesis. That was already in hand.

Then verification, by hand. Every load-bearing claim in the underlying report was **live-verified against primary sources** on 8–9 July 2026, with URL citations added inline, confidence labels applied claim by claim (**[Confirmed]**, **[Reported]**, **[Analyst speculation]**, **[Author analysis]**), and a verification log appended. The report and this memorandum were **hand-reviewed and hand-edited by Andy Kowles**. Where a source could not be machine-read, the resulting claim is marked as resting on a secondary summary rather than quietly asserted.

What is original here. The wafer-diversion model in Section 2 — the compound bit-penalty stack, its low/base/high bracketing, and the merchant-supply scenarios that follow — is **original work of Shimogoryo Base Consulting** and is published here for the first time. One input, the SLC-versus-TLC density penalty, is taken directly from the underlying report. The array-efficiency, TSV keep-out, and known-good-die penalties are the analyst's own estimates, which is precisely why they are presented as ranges rather than point figures. The tiering of companies, the ranking of opportunities, and the judgment that the actionable exposure sits with suppliers rather than memory makers are likewise the analyst's.

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> **The standard applied.** A language model is a research instrument, in the way that a screening tool or a database is a research instrument. It accelerates coverage; it does not confer understanding, and it does not carry accountability. In this memorandum the sequence was: **domain expertise** → **thesis** → **machine-assisted research at scale** → **primary-source verification** → **human editorial judgment**. Readers should weigh the analysis on that basis, and should note that the estimated inputs are labelled as estimates throughout precisely so that a reader can disagree with them and re-run the arithmetic.

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